a second MOS transistor connected in series between the supply line of a power supply voltage and ground potential, a substrate region of said second MOS transistor being permanently coupled to ground potential" and "a bias voltage supply circuit which selectively supplies a first bias voltage or a second bias voltage which are different from each other to the substrate region of the first MOS transistor, said bias voltage supply circuit comprising no more than two transistors **each having its gate coupled to receive a control signal the logical reverse of the control signal received by the other transistor**".

Independent Claim 17, as amended, requires and positively recites, A semiconductor device, comprising: "a logic circuit comprising a first MOS transistor and a second MOS transistor connected in series between the supply line of a power supply voltage and ground potential", "a first bias voltage supply circuit, comprising no more than two transistors **each having its gate coupled to receive a control signal the logical reverse of the control signal received by the other transistor**, which selectively supplies a first bias voltage or a second bias voltage which are different from each other to the substrate region of the first MOS transistor" and "a second bias voltage supply circuit, comprising no more than two transistors **each having its gate coupled to receive a control signal the logical reverse of the control signal received by the other transistor**, which selectively supplies a first bias voltage or a second bias voltage which are different from each other to the substrate region of the second MOS transistor".

In contrast, Arimoto clearly discloses that the gates of transistors Q7 and Q8 of 10b concurrently receive the SAME control signal – NOT logically reversed control signals. Similarly, transistors Q13 and Q14 of 11b currently receive the SAME control signal – NOT logically reversed control signals.

In order that the rejection of any of Claims 1-33 be sustainable, it is fundamental that "each and every element as set forth in the claim be found, either expressly or inherently described, in a single prior art reference." Verdegall Bros. v. Union Oil Co. of California, 2

USPQ2d 1051, 1053 (Fed. Cir. 1987). See also, Richardson v. Suzuki Motor Co., 9 USPQ2d 1913, 1920 (Fed. Cir. 1989), where the court states, "The identical invention must be shown in as complete detail as is contained in the ... claim".

Furthermore, "all words in a claim must be considered in judging the patentability of that claim against the prior art." In re Wilson, 424 F.2d 1382, 1385, 165 USPQ 494, 496 (CCPA 1970).

From the discussion above, it is apparent that independent Claims 1, 8 and 17, as amended, are not anticipated by Arimoto. Moreover, the Examiner has provided no evidence from the prior art that would lead one having ordinary skill in the art to re-engineer the Arimoto device to have the gates of transistors Q7 and Q8 receive logically reversed control signals, without the improper hindsight provided by Applicant's disclosure. Similarly, the Examiner has provided no evidence from the prior art that would lead one having ordinary skill in the art to re-engineer the Arimoto device to have the gates of transistors Q13 and Q14 receive logically reversed control signals, without the improper hindsight provided by Applicant's disclosure

Claims 2-7, 9-16, and 18-27 stand allowable as depending, directly or indirectly, from allowable Claim 1 and including further limitations not taught or suggested by the references of record.

Claim 2 further defines the semiconductor device of Claim 1, wherein the bias voltage supply circuit includes a first MOS transistor connected between a first voltage supply line and a bias voltage supply line and a second MOS transistor connected between a second voltage supply line and the bias voltage supply line, and said first or second bias voltage is output from the bias voltage supply line by turning on the first MOS transistor or second MOS transistor. The Arimoto reference fails to teach or suggest this further limitation in combination with the other requirements of Claim 1.

Claim 3 further defines the semiconductor device of Claim 2, wherein the MOS transistor of the logic circuit is connected to the first voltage supply line. The Arimoto reference fails to teach or suggest this further limitation in combination with the other requirements of Claim 2.

Claim 4 further defines the semiconductor device of Claim 3, wherein the MOS transistor of the logic circuit and the first MOS transistor and second MOS transistor are PMOS transistors. The Arimoto reference fails to teach or suggest this further limitation in combination with the other requirements of Claim 3.

Claim 5 further defines the semiconductor device of Claim 4, wherein the logic circuit includes an NMOS transistor connected between the PMOS transistor and a third voltage supply line. The Arimoto reference fails to teach or suggest this further limitation in combination with the other requirements of Claim 4.

Claim 6 further defines the semiconductor device of Claim 1, wherein the first bias voltage is lower than the second bias voltage. The Arimoto reference fails to teach or suggest this further limitation in combination with the other requirements of Claim 1.

Claim 7 further defines the semiconductor device of Claim 1, further including at least one additional logic circuit coupled to the bias voltage supply circuit. The Arimoto reference fails to teach or suggest this further limitation in combination with the other requirements of Claim 1.

Claim 9 further defines the semiconductor device of Claim 8, wherein the first MOS transistor is a PMOS transistor and the second MOS transistor is an NMOS transistor. The Arimoto reference fails to teach or suggest this further limitation in combination with the other requirements of Claim 8.

Claim 10 further defines the semiconductor circuit of Claim 8, wherein the first bias voltage is lower than the second bias voltage. The Arimoto reference fails to teach or suggest this further limitation in combination with the other requirements of Claim 8.

Claim 11 further defines the semiconductor circuit of Claim 8, wherein the first MOS transistor has a lower threshold voltage than said second MOS transistor. The

Arimoto reference fails to teach or suggest this further limitation in combination with the other requirements of Claim 8.

Claim 12, as amended, further defines the semiconductor circuit of Claim 8, wherein the first bias voltage is lower than the supply line voltage. The Arimoto reference fails to teach or suggest this further limitation in combination with the other requirements of Claim 8.

Claim 13, as amended, further defines the semiconductor circuit of Claim 8, wherein the bias voltage supply circuit includes a third MOS transistor connected between a first voltage supply line and a bias voltage supply line and a fourth MOS transistor connected between a second voltage supply line and the bias voltage supply line, and said first or second bias voltage is output from the bias voltage supply line by turning on the first MOS transistor or second MOS transistor. The Arimoto reference fails to teach or suggest this further limitation in combination with the other requirements of Claim 8.

Claim 14, as amended, further defines the semiconductor circuit of Claim 13, wherein the first MOS transistor of the logic circuit is connected to the first voltage supply line. The Arimoto reference fails to teach or suggest this further limitation in combination with the other requirements of Claim 13.

Claim 15, as amended, further defines the semiconductor circuit of Claim 14, wherein the first MOS transistor of the logic circuit and the third MOS transistor and fourth MOS transistor are PMOS transistors. The Arimoto reference fails to teach or suggest this further limitation in combination with the other requirements of Claim 14.

Claim 16 further defines the semiconductor circuit of Claim 15, wherein the logic circuit includes an NMOS transistor connected between the PMOS transistor and a third voltage supply line. The Arimoto reference fails to teach or suggest this further limitation in combination with the other requirements of Claim 15.

Claim 18 further defines the semiconductor device of Claim 17, wherein the first MOS transistor is a PMOS transistor and the second MOS transistor is an NMOS

transistor. The Arimoto reference fails to teach or suggest this further limitation in combination with the other requirements of Claim 17.

Claim 19 further defines the semiconductor circuit of Claim 17, wherein the first bias voltage from the first bias supply circuit is lower than the second bias voltage from the first bias supply circuit. The Arimoto reference fails to teach or suggest this further limitation in combination with the other requirements of Claim 17.

Claim 20 further defines the semiconductor circuit of Claim 17, wherein the first bias voltage from the second bias supply circuit is lower than the second bias voltage from the second bias supply circuit. The Arimoto reference fails to teach or suggest this further limitation in combination with the other requirements of Claim 17.

Claim 21 further defines the semiconductor circuit of Claim 17, wherein the first MOS transistor has a lower threshold voltage than said second MOS transistor. The Arimoto reference fails to teach or suggest this further limitation in combination with the other requirements of Claim 17.

Claim 22 further defines the semiconductor circuit of Claim 17, wherein the first bias voltage supply circuit includes a first MOS transistor connected between a first voltage supply line and a bias voltage supply line and a second MOS transistor connected between a second voltage supply line and the bias voltage supply line, and said first or second bias voltage is output from the bias voltage supply line by turning on the first MOS transistor or second MOS transistor. The Arimoto reference fails to teach or suggest this further limitation in combination with the other requirements of Claim 17.

Claim 23, as amended, further defines the semiconductor circuit of Claim 17, wherein the second bias voltage supply circuit includes a third MOS transistor connected between the substrate of the second MOS transistor of the logic circuit and ground potential and a fourth MOS transistor connected between the substrate of the second MOS transistor of the logic circuit and a first bias supply line. The Arimoto reference fails to teach or suggest this further limitation in combination with the other requirements of Claim 17.

Claim 24 further defines the semiconductor circuit of Claim 17, wherein: "the first bias voltage supply circuit includes a first MOS transistor connected between a first voltage supply line and a bias voltage supply line and a second MOS transistor connected between a second voltage supply line and the bias voltage supply line, and said first or second bias voltage is output from the bias voltage supply line by turning on the first MOS transistor or second MOS transistor" and " the second bias voltage supply circuit includes a third MOS transistor connected between the substrate of the second MOS transistor of the logic circuit and ground potential and a fourth MOS transistor connected between the substrate of the second MOS transistor of the logic circuit and a third bias supply line". The Arimoto reference fails to teach or suggest this further limitation in combination with the other requirements of Claim 17.

Claim 25 further defines the semiconductor circuit of Claim 22, wherein the first and second MOS transistors of the first bias voltage supply circuit are PMOS transistors. The Arimoto reference fails to teach or suggest this further limitation in combination with the other requirements of Claim 22.

Claim 26 further defines the semiconductor circuit of Claim 23, wherein the first and second MOS transistors of the second bias voltage supply circuit are NMOS transistors. The Arimoto reference fails to teach or suggest this further limitation in combination with the other requirements of Claim 23.

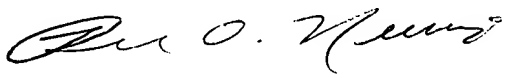
Claim 27 further defines the semiconductor circuit of Claim 22, wherein the first and second MOS transistors of the first bias voltage supply circuit are PMOS transistors and the first and second MOS transistors of the second bias voltage supply circuit are NMOS transistors. The Arimoto reference fails to teach or suggest this further limitation in combination with the other requirements of Claim 22.

An amendment after a final rejection should be entered when it will place the case either in condition for allowance or in better form for appeal. 37 C.F.R. 1.116; MPEP 714.12. This amendment places the case in condition for allowance. At a minimum, the amendment should be entered since it reduces the issues for appeal by overcoming the objections to Claim 23. The newly cited Arimoto reference necessitates the need for the proposed amendment. The amendment introduces no new matter.

Attached hereto is a marked-up version of the changes made to the specification and claims by the current amendment. The attached page is captioned **"Version with markings to show changes made."**

Claims 1-27 stand allowable over the cited art and the application is in allowable form. Applicant respectfully requests allowance of the application as the earliest possible date.

Respectfully submitted,



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VERSION WITH MARKINGS TO SHOW CHANGES MADE

IN THE CLAIMS – (marked-up version):

1. (twice amended) A semiconductor device, comprising:

a logic circuit, which includes a MOS transistor, and

a bias voltage supply circuit, comprising no more than two transistors each having its gate coupled to receive a control signal the logical reverse of the control signal received by the other transistor, which selectively supplies a first bias voltage or a second bias voltage which are different from each other to the substrate region of the MOS transistor.

2. The semiconductor device of Claim 1, wherein the bias voltage supply circuit includes a first MOS transistor connected between a first voltage supply line and a bias voltage supply line and a second MOS transistor connected between a second voltage supply line and the bias voltage supply line, and said first or second bias voltage is output from the bias voltage supply line by turning on the first MOS transistor or second MOS transistor.

3. The semiconductor device of Claim 2, wherein the MOS transistor of the logic circuit is connected to the first voltage supply line.

4. The semiconductor device of Claim 3, wherein the MOS transistor of the logic circuit and the first MOS transistor and second MOS transistor are PMOS transistors.

5. The semiconductor device of Claim 4, wherein the logic circuit includes an NMOS transistor connected between the PMOS transistor and a third voltage supply line.

6. The semiconductor device of Claim 1, wherein the first bias voltage is lower than the second bias voltage.

7. The semiconductor device of Claim 1, further including at least one additional logic circuit coupled to the bias voltage supply circuit.

8. (twice amended) A semiconductor device, comprising:

a logic circuit comprising a first MOS transistor and a second MOS transistor connected in series between the supply line of a power supply voltage and ground potential, a substrate region of said second MOS transistor being permanently coupled to ground potential; and

a bias voltage supply circuit which selectively supplies a first bias voltage or a second bias voltage which are different from each other to the substrate region of the first MOS transistor, said bias voltage supply circuit comprising no more than two transistors each having its gate coupled to receive a control signal the logical reverse of the control signal received by the other transistor.

9. The semiconductor device of Claim 8, wherein the first MOS transistor is a PMOS transistor and the second MOS transistor is an NMOS transistor.

10. The semiconductor circuit of Claim 8, wherein the first bias voltage is lower than the second bias voltage.

11. The semiconductor circuit of Claim 8, wherein the first MOS transistor has a lower threshold voltage than said second MOS transistor.

12. The semiconductor circuit of Claim 8, wherein the first bias voltage is lower than the supply line voltage.

13. The semiconductor circuit of Claim 8, wherein the bias voltage supply circuit includes a third MOS transistor connected between a first voltage supply line and a bias voltage supply line and a fourth MOS transistor connected between a second voltage supply line and the bias voltage supply line, and said first or second bias voltage is output

from the bias voltage supply line by turning on the first MOS transistor or second MOS transistor.

14. The semiconductor circuit of Claim 13, wherein the first MOS transistor of the logic circuit is connected to the first voltage supply line.

15. The semiconductor circuit of Claim 14, wherein the first MOS transistor of the logic circuit and the third MOS transistor and fourth MOS transistor are PMOS transistors.

16. The semiconductor circuit of Claim 15, wherein the logic circuit includes an NMOS transistor connected between the PMOS transistor and a third voltage supply line.

17. (twice amended) A semiconductor device, comprising:

a logic circuit comprising a first MOS transistor and a second MOS transistor connected in series between the supply line of a power supply voltage and ground potential;

a first bias voltage supply circuit, comprising no more than two transistors each having its gate coupled to receive a control signal the logical reverse of the control signal received by the other transistor, which selectively supplies a first bias voltage or a second bias voltage which are different from each other to the substrate region of the first MOS transistor; and

a second bias voltage supply circuit, comprising no more than two transistors each having its gate coupled to receive a control signal the logical reverse of the control signal received by the other transistor, which selectively supplies a first bias voltage or a second bias voltage which are different from each other to the substrate region of the second MOS transistor.

18. The semiconductor device of Claim 17, wherein the first MOS transistor is a PMOS transistor and the second MOS transistor is an NMOS transistor.

19. The semiconductor circuit of Claim 17, wherein the first bias voltage from the first bias supply circuit is lower than the second bias voltage from the first bias supply circuit.

20. The semiconductor circuit of Claim 17, wherein the first bias voltage from the second bias supply circuit is lower than the second bias voltage from the second bias supply circuit.

21. The semiconductor circuit of Claim 17, wherein the first MOS transistor has a lower threshold voltage than said second MOS transistor.

22. The semiconductor circuit of Claim 17, wherein the first bias voltage supply circuit includes a first MOS transistor connected between a first voltage supply line and a bias voltage supply line and a second MOS transistor connected between a second voltage supply line and the bias voltage supply line, and said first or second bias voltage is output from the bias voltage supply line by turning on the first MOS transistor or second MOS transistor.

23. (amended) The semiconductor circuit of Claim 17, wherein the second bias voltage supply circuit includes a third MOS transistor connected between the substrate of the second MOS transistor of the logic circuit and ground potential and a <u>fourth</u> [second] MOS transistor connected between the substrate of the second MOS transistor of the logic circuit and a first bias supply line.

24. The semiconductor circuit of Claim 17, wherein:

the first bias voltage supply circuit includes a first MOS transistor connected between a first voltage supply line and a bias voltage supply line and a second MOS transistor connected between a second voltage supply line and the bias voltage supply line, and said first or second bias voltage is output from the bias voltage supply line by turning on the first MOS transistor or second MOS transistor; and

the second bias voltage supply circuit includes a third MOS transistor connected between the substrate of the second MOS transistor of the logic circuit and ground potential and a fourth MOS transistor connected between the substrate of the second MOS transistor of the logic circuit and a third bias supply line.

25. The semiconductor circuit of Claim 22, wherein the first and second MOS transistors of the first bias voltage supply circuit are PMOS transistors.

26. The semiconductor circuit of Claim 23, wherein the first and second MOS transistors of the second bias voltage supply circuit are NMOS transistors.

27. The semiconductor circuit of Claim 22, wherein the first and second MOS transistors of the first bias voltage supply circuit are PMOS transistors and the first and second MOS transistors of the second bias voltage supply circuit are NMOS transistors.